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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,541	10/23/2003	Jun-Ichiro Furihata	108868.01	9089

25944 7590 03/14/2005

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EXAMINER	
RHEE, JANE J	

ART UNIT	PAPER NUMBER
1745	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,541	FURIHATA ET AL.	
	Examiner	Art Unit	
	Jane Rhee	1772	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/14/2004 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2,4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (6004866) in view Taksaski (EP 0928017).

Nakano et al. discloses a bonded wafer having a base wafer is bonded to a bond wafer (col. 1 lines 33-35). Nakano et al. teaches that the base layer comprises peels which are wave-like irregularities having small heights or shallow depths in the range of 0.01-0.1um in peak to valley value (col. 2 lines 52-54) that are created by irregularities on the rear surface of a wafer or the figure of the surface of a polishing plate which is in contact with the rear surface of the wafer, being transferred onto the front surface of the

wafer during the polishing of the wafer and furthermore from this matter, it is considered that the thickness irregularity of the thinned layer of the bonded wafer is caused due to being not able to completely remove the peels of the wafer which are created during a polishing step (col. 2 lines 40-50). However, Nakano et al. teaches to remove the irregularities by using a double polishing method to absorb the irregularities on the rear surface (col. 7 lines 11-21).

Nakano et al. fail to disclose a wafer comprising a maximal depth of pits is 6 micrometers or less and an average value of waviness of 0.04 micrometers or less. Nakano et al. fail to disclose the power spectrum density of the wafer is 0.5 to 10 cubic micrometer as measured by the waviness having a wavelength of 10mm.

Takashi et al. discloses a wafer comprising a maximal depth of pits is 6 micrometers or less (page 4 line 44) and an average value of waviness of 0.04 micrometers or less (page 4 line 45) for the purpose of providing a wafer with a smooth and flat etched surface that hardly cases generations of particles and contaminations such as stain, therefore the amount of stock removal in a mirror polishing step can be decreased, and the flatness of the wafer can be improved.

Nakano et al. fail to disclose a chamfered part of the base wafer is mirror surface. Takashi et al. teaches the method of chamfering, lapping, etching, mirror polishing, and cleaning (page 3 lines 1-4) wherein the pits are removed through a mirror polishing step for the purpose of decreasing the depth of the pits to a possible extent (page 5 lines 42-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time applicant's invention was made to provide Nakano et al. a chamfered part of the base that is a mirror surface in order to decrease the dept of the pits to a possible extent as taught by Takashi et al. (page 5 lines 42-44).

A bonded wafer having a base wafer wherein a back surface of the base wafer is chemically etched, a chamfered part of the base wafer is subjected to chamfering and mirror finishing to form a mirror surface, and the chemically etched back surface is subjected to acid etching following to alkali etching are process limitations, process limitations are given little or no patentable weight. The method of forming the product is not germane to the issue of patentability of the product itself. Further, when the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claim in a product-by-process claim, the burden is on the Applicant to present evidence from which the Examiner could reasonably conclude that the claimed product differs in kind from those of the prior art. *In re Brown*, 459 F.2d 531, 173 USPQ 685 (CCPA 1972); *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974). This burden is NOT discharged solely because the product was derived from a process not known to the prior art. *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974).

Furthermore, Takashi et al. discloses the method of chamfering, lapping, etching, mirror polishing, and cleaning (page 3 lines 1-4), also note that example 1 of Takashi employs similar process parameters as example 1 of the instant application. Therefore, the product of Takashi et al. would have the same properties as the claimed product,

including the power spectrum density of 0.5 to 10 cubic micrometer as measured by the waviness having a wavelength of 10mm.

Response to Arguments

3. Applicant's arguments filed 12/14/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that Nakano does not teach or suggest that a chamfered part of the wafer to be mirror polished, Takashi et al. teaches the method of chamfering, lapping, etching, mirror polishing, and cleaning (page 3 lines 1-4) wherein the pits are removed through a mirror polishing step for the purpose of decreasing the depth of the pits to a possible extent (page 5 lines 42-44). Therefore, it would have been obvious to one having ordinary skill in the art at the time applicant's invention was made to provide Nakano et al. a chamfered part of the base that is a mirror surface in order to decrease the dept of the pits to a possible extent as taught by Takashi et al. (page 5 lines 42-44).

In response to applicant's argument that Nakano does not teach that such a mirror polished chamfered part would accordingly improve manufacturing yield and reduce cost, applicant did not claim that a mirror polished chamfered part would accordingly improve manufacturing yield and reduce cost, and furthermore, Takashi teaches the a chamfered part of the base that is mirror surface in order to decrease the depth of the pits to a possible extend (page 5 lines 42-44).

In response to applicant's argument that Takashi fail to teach that a chamfered part of the base wafer is mirror polished, Takashi et al. teaches the method of

chamfering, lapping, etching, mirror polishing, and cleaning (page 3 lines 1-4) wherein the pits are removed through a mirror polishing step for the purpose of decreasing the depth of the pits to a possible extent (page 5 lines 42-44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jane Rhee whose telephone number is 571-272-1499. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Harold Pyon can be reached on 571-272-1498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jane Rhee
February 18,2005

PATRICK JOSEPH RYAN
SUPERVISORY PATENT EXAMINER